WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising two or more different memory cell arrays formed on a chip, at least two different ones of said memory cell arrays being formed at different positions to each other in the vertical direction relative to said chip.

2. A semiconductor memory device according to claim 1, wherein at least a wiring conductor layer is interposed between said vertically formed memory cell arrays.

3. A semiconductor memory device according to claim 1, wherein data is transferred between said two vertically formed different memory arrays.

4. A semiconductor memory device according to claim 1, wherein when a memory cell array that takes a longer time to rewrite data, as one of said two vertically provided memory cell arrays, transfers its stored data to the outside, said stored data is transferred through the other memory cell array to the outside.

5. A semiconductor memory device according to claim 1, wherein the storage capacity of a memory cell array that takes a shorter time to rewrite data, as one of said two vertically provided memory cell arrays, is half that of the other memory cell array.

6. A semiconductor memory device according to claim 1, wherein one of said two vertically provided memory cell arrays has the function of a sense

amplifier for the other memory cell array.

7. A semiconductor memory device according to claim 1, wherein the upper one of said two vertically provided memory cell arrays does not need refresh operation, the lower one thereof needs refresh operation, and a logic circuit is provided at the same height as is the lower memory.

8. A semiconductor memory device comprising:

a plurality of matrix-shape arranged semiconductor memory cells each having source and drain regions provided on an insulator film and connected together through a semiconductor, a control electrode, and at least one memory region surrounded by a potential barrier into or from which charges are injected or discharged by applying a voltage between said control electrode and said source, said drain so as to store data by utilizing the fact that the conductance between said source and drain is changed depending upon the amount of charges accumulated in said memory region; and

a plurality of transistors provided on a substrate surface, some of said matrix-shaped semiconductor memory cells and some of said plurality of transistors being formed substantially at different levels in the vertical direction.

9. A semiconductor memory device according to claim 8, wherein said semiconductor for connecting said source and drain of said semiconductor cell is made of

polycrystalline silicon.

10. A semiconductor memory device according to claim 8, wherein said memory region of said semiconductor memory cell is formed of at least one minute crystal pellet of 10 nm or below in shorter diameter.

11. A semiconductor memory device according to claim 8, wherein said plurality of transistors provided on said substrate surface constitute a sense amplifier or a part thereof.

12. A semiconductor memory device according to claim 11, wherein said sense amplifier is arranged in a two-dimensional manner.

13. A semiconductor memory device according to claim 8, further comprising data lines and word lines for controlling said semiconductor memory cells, wherein said sense amplifier relative to a pair of adjacent data lines is not arranged in parallel to said word lines, but arranged to shift in parallel to said data lines.

14. A semiconductor memory device according to claim 8, wherein a metal conductor layer is provided between said semiconductor memory cells and said transistors formed on said substrate surface.

15. A data processor device comprising:

an authentication function for judging access right;

a nonvolatile memory cell array formed on an

insulator film of a chip; and

a conductor layer provided between a logic circuit for said authentication and said nonvolatile memory.

16. A data processor device according to claim 15, wherein said nonvolatile memory stores at least part of authentication information or authentication program.

17. A data processor device according to claim 15, further comprising another nonvolatile memory cell array formed by a production process different from the process by which said fast-mentioned nonvolatile memory cell array is formed, wherein authentication information or authentication program is dispersedly stored in said two different nonvolatile memory cell arrays.